

File 351:Derwent WPI 1963-2001/UD,UM &UP=200201

(c) 2002 Derwent Info Ltd

**\*File 351: Price changes as of 1/1/02. Please see HELP RATES 351.**

More updates in 2002. Please see HELP NEWS 351.

Set Items Description

?e pn=de 3932277

Ref	Items	Index-term
E1	1	PN=DE 3932275
E2	1	PN=DE 3932276
E3	1	*PN=DE 3932277
E4	1	PN=DE 3932278
E5	1	PN=DE 3932279
E6	1	PN=DE 3932281
E7	1	PN=DE 3932282
E8	1	PN=DE 3932283
E9	1	PN=DE 3932285
E10	1	PN=DE 3932287
E11	1	PN=DE 3932288
E12	1	PN=DE 3932289

Enter P or PAGE for more

?ss e3

S1 1 PN="DE 3932277"

?t s1/9/all

1/9/1

DIALOG(R)File 351:Derwent WPI

(c) 2002 Derwent Info Ltd. All rts. reserv.

008221833 \*\*Image available\*\*

WPI Acc No: 1990-108834/ 199015

XRAM Acc No: C90-047755

XRPX Acc No: N90-084218

**Micro-electronic semiconductor device with lattice adaptation - by  
superlattice for contact area between them and with alternative material  
removed where devices are made in one of materials**

Patent Assignee: MITSUBISHI DENKI KK (MITQ )

Inventor: HAYASHI K; SONODA T

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 3932277	A	19900405	DE 3932277	A	19890927	199015 B
JP 2094663	A	19900405	JP 88247608	A	19880930	199020
DE 3932277	C	19920709	DE 3932277	A	19890927	199228

Priority Applications (No Type Date): JP 88247608 A 19880930

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

DE 3932277 C 9 H01L-029/267

Abstract (Basic): DE 3932277 A

In a first structure on a semiconductor substrate (1, 4) a super lattice (3) is deposited to allow depositions of a second semiconductor (5, 6) with a different composition and lattice constant. The structure features areas (7) in which the substrate material has been removed and areas (4') in which the super lattice and layers above have been removed. The active devices (9,10) are preferably constructed in the areas

where only 1 of the materials remains. Where the 2 materials overlap the super lattice remains present to ensure adaptation. The substrate (1, 4) is pref. Si, the second semiconductor material is pref. GaAs (5, 6). Also claimed is a structure using a Si substrate in which an insulating layer with a suitable lattice constant, e.g. CaF<sub>2</sub>, is formed between the bulk (1) and the epitaxial layer (4). The first material is pref. a solar cell and the second material pref. forms a laser diode. Also claimed is the first structure with the addition of a layer of heat conductive material (11) coating the inside of the opening (7) etched in the substrate. Also claimed is a structure as above with, instead of the heat dissipating layer, further layers of the second semiconductor are grown epitaxially and a device is formed in them. A pref. process flow for mfr. is also claimed.

USE/ADVANTAGE - The method allows the use of semiconductor materials with different lattice constants in a combined device without incurring high mismatch related defects in the surfaces, i.e. showing 10-10 power 4 defects/cm<sup>2</sup> instead of the 10 power 6/cm<sup>2</sup> level currently achieved. This allows similar characteristics to be achieved in the devices as in single material devices. The structures are used for the mfr. of opto-electronic and electronic devices. (10pp Dwg.No.1d,e,f/5)

Abstract (Equivalent): DE 3932277 C

Semiconductor structure comprises a substrate (1, 4) of a first semiconductor material, an over-lattice (3) deposited on the substrate, and a semiconductor body (5, 6) of a second semiconductor material deposited on the over-lattice. The lattice constant of the second semiconductor material is different from that of the first. There is at least one relieved region (7) in the semiconductor substrate, exposing the surface of the over-lattice and at least one first semiconductor unit or device (10) in the semiconductor body above this region.

USE/ADVANTAGE - Fewer defects in the semiconductor body. It is suitable for semiconductor techniques.

(Dwg.1e/5)

Title Terms: MICRO; ELECTRONIC; SEMICONDUCTOR; DEVICE; LATTICE; ADAPT; SUPERLATTICE; CONTACT; AREA; ALTERNATIVE; MATERIAL; REMOVE; DEVICE; MADE; ONE; MATERIAL

Derwent Class: L03; U11; U12; U13; V08

International Patent Class (Main): H01L-029/267

International Patent Class (Additional): H01L-021/20; H01L-023/36;

H01L-027/09; H01L-029/26; H01L-029/784; H01L-031/0304; H01L-031/04;

H01S-003/19

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L03-E05B; L04-C01; L04-E03B

Manual Codes (EPI/S-X): U11-C18B; U12-A01B; U12-A02A2; U12-E01; U13-D04;

V08-A04A

?

?b345

07jan02 13:42:49 User211886 Session D578.2

Sub account: STK00045PUS/STUNKEL

\$7.07 0.273 DialUnits File351

\$4.92 1 Type(s) in Format 9

\$4.92 1 Types

\$11.99 Estimated cost File351

\$0.19 TELNET

\$12.18 Estimated cost this search

\$12.26 Estimated total session cost 0.463 DialUnits

File 345:Inpadoc/Fam.& Legal Stat 1968-2001/UD=200151

(c) 2002 EPO

Set	Items	Description
---	-----	-----
?ss pn=de 3932277		
S1	1	PN=DE 3932277
?t s1/9/all		

1/9/1  
 DIALOG(R)File 345:Inpadoc/Fam.& Legal Stat  
 (c) 2002 EPO. All rts. reserv.

9189266  
 Basic Patent (No,Kind,Date): DE 3932277 A1 900405 <No. of Patents: 003>

# PATENT FAMILY:

## GERMANY (DE)

Patent (No,Kind,Date): DE 3932277 A1 900405  
 HALBLEITEREINRICHTUNG UND VERFAHREN ZU IHRER HERSTELLUNG (German)  
 Patent Assignee: MITSUBISHI ELECTRIC CORP (JP)  
 Author (Inventor): SONODA TAKUJI (JP); HAYASHI KAZUO (JP)  
 Priority (No,Kind,Date): JP 88247608 A 880930  
 Applic (No,Kind,Date): DE 3932277 A 890927  
 IPC: \* H01L-029/267; H01L-021/20; H01L-023/36; H01L-029/78;  
 H01L-031/04; H01S-003/19  
 CA Abstract No: ; 113(14)124804M  
 Derwent WPI Acc No: ; C 90-108834  
 Language of Document: German  
 Patent (No,Kind,Date): DE 3932277 C2 920709  
 HALBLEITERSTRUKTUR (German)  
 Patent Assignee: MITSUBISHI ELECTRIC CORP (JP)  
 Author (Inventor): SONODA TAKUJI (JP); HAYASHI KAZUO (JP)  
 Priority (No,Kind,Date): JP 88247608 A 880930  
 Applic (No,Kind,Date): DE 3932277 A 890927  
 Filing Details: DE C2 D2 Grant of a patent after examination process  
 IPC: \* H01L-029/267; H01L-021/20; H01L-023/36; H01L-029/784;  
 H01L-031/0304; H01S-003/19  
 CA Abstract No: \* 113(14)124804M  
 Derwent WPI Acc No: \* C 90-108834  
 JAPIO Reference No: \* 140292E000122  
 Language of Document: German

## GERMANY (DE)

### Legal Status (No,Type,Date,Code,Text):

DE 3932277	P	880930	DE AA	PRIORITY (PATENT APPLICATION)
			(PRIORITAET	(PATENTANMELDUNG))
			JP 88247608	A 880930
DE 3932277	P	890927	DE AE	DOMESTIC APPLICATION (PATENT APPLICATION)
			(INLANDSANMELDUNG	(PATENTANMELDUNG))
			DE 3932277	A 890927
DE 3932277	P	900405	DE A1	LAYING OPEN FOR PUBLIC INSPECTION
			(OFFENLEGUNG)	
DE 3932277	P	900405	DE OP8	REQUEST FOR EXAMINATION AS TO PARAGRAPH 44 PATENT LAW
			(PRUEFUNGSANTRAG	GEM. PAR. 44 PATG. IST GESTELLT)
DE 3932277	P	920709	DE D2	GRANT AFTER EXAMINATION
			(PATENTERTEILUNG NACH DURCHFUEHRUNG DES	PRUEFUNGSVERFAHRENS)
DE 3932277	P	930114	DE 8364	NO OPPOSITION DURING TERM OF OPPOSITION
			(EINSPRUCHSFRIST ABGELAUFEN OHNE	DASS EINSPRUCH ERHOBEN WURDE)

DE 3932277

P

960125

DE 8320

WILLINGNESS TO GRANT LICENSES  
DECLARED (PARAGRAPH 23) (LIZENZBEREITSCHAFT  
ERKLAERT (PAR. 23))

JAPAN (JP)

Patent (No,Kind,Date): JP 2094663 A2 900405

SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF (English)

Patent Assignee: MITSUBISHI ELECTRIC CORP

Author (Inventor): SONODA TAKUJI; HAYASHI KAZUO

Priority (No,Kind,Date): JP 88247608 A 880930

Applic (No,Kind,Date): JP 88247608 A 880930

IPC: \* H01L-027/095; H01L-021/20; H01S-003/18

JAPIO Reference No: ; 140292E000122

Language of Document: Japanese

?logoff